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Fully Parallel ASIC Interface for a 3 Dimensional Processor for Image Convolution

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Introduction: Real time image processing for recognition of objects and patterns from fast-frame image data requires extremely high speed convolution (inner-product) of image segments with multiple kernels, fundamentally a computation-intensive operation. JPL is developing a 3-dimensional neural processing module (NPM) [1] as a high speed convolver to solve spatio-temporal object recognition problems in fully parallel fashion. It would raster a 256x256 image with a 64x64 window and perform inner product (multiply-accumulate) convolution operations with a set of 64 independent kernels (each 64x64) in parallel at a rate of 64 frames per second resulting in over one tera (1012) [multiply-accumulate] operations per second. A technical challenge for such an architecture is the feeding of one 64x64 image segment every 250ns to the NPM cube. To that end, this paper describes the JPL-developed column loading input chip (CLIC) fabricated in 1 μm CMOS, mated to the NPM cube with 4096 (64x64) iridium bumps, interfaced with a frame grabber for its image input. Thus, CLIC would provide 4096 analog inputs to the NPM cube for image convolution every 250 nanoseconds (at a rate of -16 gigapixels/s).

Neural Processor: The 3-D Neural Processor (NP) consists of a CLIC mated to the NPM cube as shown schematically in Figure 1, with a picture of the actual assembly along with the mother board shown in Figure 2. The CLIC is capable of acquiring rastered 8-bit resolution digital image data, 64x64 window at a time from (say) an image buffer, converting the digital window to an analog array of signals, and feeding these 4096 signals in parallel to the NPM. The NPM, consisting of 64 chips, each with an array of 64x64, 8-bit multiplying digital to analog converters (MDAC), would receive this image, and perform a set of inner products with a total of 64 templates, each of 64x64 size, all in parallel, every 250 ns.

The CLIC is designed to contain three peripheral shift registers (up, down, or right shifts) which (one at a time) receive a 64 byte column or row segment from the image buffer. A 64x64 array of shift registers (SRs) receives and shifts data either column-wise (right only) or row-wise (either up or down). SRS are connected to individual 64x64 array of MDACS which have their outputs brought to an iridium bump, mated to the NPM cube [2].

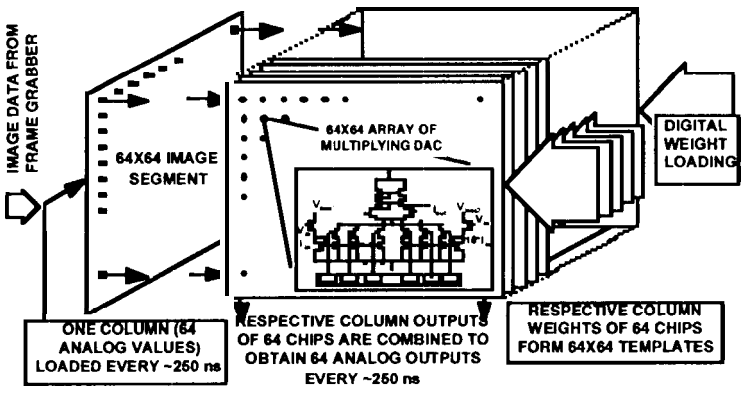

Figure 1. A schematic of the Neural Processor with CLIC and NPM for high speed image convolution.

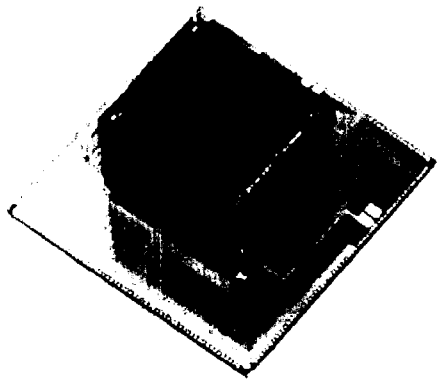

Figure 2. A photograph of NP with CLIC mated at top.

Results and Discussion: Wafers with CLIC die were fabricated in 1 μm CMOS. Some die were packaged for characterization and testing. Others were tested as die mounted on specially fabricated die-jig with probes prior to mating with NPM cube. 3-D packaging was done by Irvine Sensors Corporation (Fig. 2). Three such 3D processors have been assembled and are currently under test. The digital circuitry was tested and validated for up to 50 MHz operation and the analog MDACS settled in about 200 ns with output buffers in circuit, consistent with the design specifications [2]. Circuit design details and performance results of CLIC, in conjunction with the overall NPM operation, as a dedicated ultra-high-speed image processor will be presented.

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References:

1. T.A. Duong, et al. "Analog 3-D Neuroprocessor for Fast Frame Focal Plane Image processing" *Simulation*, Vol. 65, No. 1, pp. 11-25, July 1995.
2. T.A. Duong, et al. "64x64 Analog Input Array for 3-Dimensional Neural Network Processor," EURAP 97 Conference at Marseilles, France, March 1997.